DESIGN GUIDELINES

Apollo System on Chip

Ultra-Low Power Apollo SoC Family

A-SOCAP1-DGGA01EN v1.1

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Revision History

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1.0	February 2017	Initial release
1.1	January 5, 2023	Updated document template

Reference Documents

Document ID	Description

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SECTION

1 Introduction

This document is a compilation of detailed design guidelines for the Apollo system on chip (SoC).

SECTION

2

Design Guidelines Summary List

A summary of the design guidelines described in this document is listed below. This lists each design guideline by reference number and title, and a link to its detailed information.

- *General Power Considerations, pg 9*
- *32.768 kHz Crystal Selection and Calibration, pg 12*
- *Reset Design Considerations, pg 15*
- *ADC Input Characteristics, pg 16*
- *Debug Connections, pg 18*
- *IOM/IOS Connections, pg 20*

SECTION

3

Detailed Design Guidelines

This section contains the design guidelines. Information covered in each design guideline includes at minimum the following:

- **Design Guideline Reference Number and Title** – Lists reference number and title of the design guidelines topic
- **Overview** – Provides an overview of what is addressed in the design guidelines
- **Applicable Silicon Revisions** – Specifies the silicon revisions to which the design guideline applies
- **Application Impact** – Describes the impact of the addressed issue(s) on a user application
- **Guidelines** – Provides details of the design guidelines

3.1 General Power Considerations

3.1.1 Overview

These design guidelines describe device-level power requirements for Apollo. Consult the Electrical Characteristics chapter of the Apollo Datasheet for operating specifications, and ensure that these specifications are always met.

3.1.2 Applicable Silicon Revisions

These design recommendations apply to all versions and packages of Apollo silicon, APOLLO512-xxx.

3.1.3 Application Impact

The power guidelines are intended to ensure reliable low-power operation. Not adhering to these recommendations may result in unnecessary power consumption and, in some cases, unreliable operation of the Apollo SoC.

3.1.4 Guidelines

3.1.4.1 Power Supply Decoupling

Minimum required power supply decoupling is:

- 1 µF on V_{DDP}
- 0.1 µF on V_{DDA}
- 0.1 µF on V_{DDH}

Although the minimum decoupling capacitance on V_{DDP} is 1 µF, it is recommended to include a larger capacitor in the range of 2 µF to 10 µF depending on the transient loads in the system. The Apollo V_{DDP} input has a maximum allowed slew rate of 2 kV/s, and this extra decoupling capacitance on V_{DDP} may be required if there are high transient loads on the V_{DDP} rail.

This capacitance can be adjusted down to the lowest necessary to prevent the VDDP slew rate from exceeding the 2 kV/s limit for Apollo (but should not be reduced below 1 µF).

3.1.4.2 DC-DC Buck - Inductors and Capacitors

Apollo features two built-in Buck converters optimized for a low-power environments, featuring ultra-low quiescent current and an integrated power switch. Therefore, only an external inductor and capacitor are needed for each converter to enable very high efficiency power input for the SoC core, SRAM, Flash memory, analog blocks and digital logic.

To ensure best performance across process, voltage and temperature, voltage and temperature, additional capacitance is needed at the VOUT1 Buck converter output to help reduce ripple. Compared to older Apollo example schematics, the VOUT1 output capacitor must be increased from 1 µF to 2 µF. Using a standard capacitor value of 2.2 µF is also acceptable. See Figure 3-1 on page 11 for an updated Buck converter example schematic.

- 2 µF on VOUT1
- 1 µF on VOUT2

Buck mode operation provides much higher power efficiency in active mode but requires the use of inductors.

The same size and type is recommended for both VOUT1 (core) inductor and VOUT2 (memory) inductor. There is an option for choosing the size and type of these inductors. If a smaller footprint is required in the design at the expense of slightly higher current draw, then the recommendation is a 0603 SMT package from Taiyo Yuden:

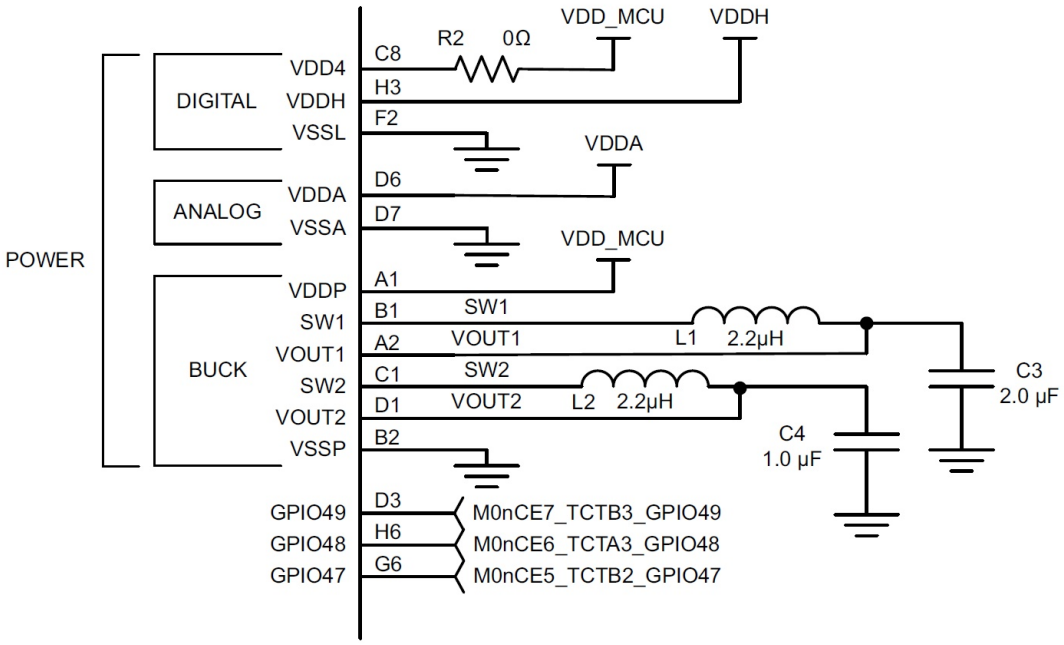
MBKK1608T2R2M
(2.2 µH, .345 Ω, 750 mA current rating, 520 mA saturation current)

If better buck efficiency (up to 5% lower current draw) is needed at the expense of a larger package, then the recommendation is a 0806 SMT package from Bourns:

SRN2010TA-2R2M
(2.2 µH, .145 Ω, 1.2 A current rating, 1.26A saturation current)

If another pair of inductors is selected, it is recommended to ensure 500 mA or higher saturation current for both outputs.

Figure 3-1: Updated Buck Converter Schematic, Showing C3 Value as 2.0 µF



3.1.4.3 Input Supply Voltage and Rising POR Threshold

The Apollo device is designed to work with input power supplies between 1.8 V and 3.8 V, after a power-on reset condition has been de-asserted. However, to de-assert the power-on reset condition, a supply voltage higher than the POR threshold of ≥2.05 V must be applied to the device for at minimum 100 ms. After that condition is satisfied, system reset is de-asserted and normal SoC operation proceeds.

Typical power supply designs do not allow for a short 100 ms voltage pulse of ≥2.05 V, followed by a steady-state value of around 1.8 V. Therefore, Ambiq recommends that most customers use a voltage supply at minimum of 2.1 V to power the Apollo SoC, unless such a voltage sequence is possible in their design.

All Apollo supplies must be provided the same voltage such that $V_{DDP} = V_{DDH} = V_{DDA}$.

3.2 32.768 kHz Crystal Selection and Calibration

3.2.1 Overview

These design guidelines outline crystal selection considerations and crystal calibration during manufacturing for on an Apollo design.

3.2.2 Applicable Silicon Revisions

These design guidelines apply to all versions and packages of Apollo silicon, APOLLO512-xxx.

3.2.3 Application Impact

Proper selection of the crystal and design of the crystal circuit should be made to ensure required clock accuracy and reliable operation.

3.2.4 Guidelines

3.2.4.1 32.768 kHz Crystal and Load Capacitors

The Apollo SoC clock generator module includes a high-precision crystal-controlled oscillator that works in conjunction with an external 32.768 kHz tuning fork crystal. The crystal oscillator includes a distributed digital calibration function that can be used to calibrate the 16 kHz level of the internal SoC clock divider chain to within ±1 ppm accuracy.

The crystal oscillator is designed to run without the use of external load capacitors, and use the digital calibration function to create a highly accurate clock for internal use. Not using external load capacitors significantly increases oscillator allowance, and allows for a reduction in crystal bias current, which results in lower power consumption. Lower power consumption is often most beneficial when the SoC is in deep sleep mode, but needs to keep the crystal oscillator running as an accurate time source for the RTC module.

The following parameters should be used for the crystal and the crystal circuit:

1. Crystal load capacitance rating: 0 – 12 pF
2. Crystal ESR rating: 0 – 90 kΩ max
3. No external load capacitors on the board

   4 pF or smaller external load capacitor[1] (4.7 pF total external capacitance) if lowppm non-calibrated 32 kHz clock is required.

Crystals which have been tested with the Ambiq crystal circuit are the following:

- Abracon: ABS07-32.768KHZ-7-T, ABS06-32.768KHZ-9-T, ABS25.32.768KHZ-T
- Epson: C-002RX, FC-135, FC-12D, FC-12M
- Microcrystal: CC7V-T1A, CM7V-T1A

All crystals were tested with no external load capacitors.

General Notes:

1. Ambiq typically generates an oscillator allowance of at least 500 kΩ following the guidelines above. Increasing the load capacitance on the XI/XO pins will decrease the oscillator allowance, and using crystals with a higher ESR will reduce the oscillator allowance margin.
2. Common size crystals (3.2 mm x 1.5 mm) generally have a maximum ESR rating of 70 kΩ. The very small 2.0 mm x 1.2 mm crystals generally have a maximum ESR of 90 kΩ, but some crystal vendors, such as Abracon, Epson, or Microcrystal, will have some of the smaller crystals with lower ESR.
3. No external load capacitance is required because the RTC clock source can be digitally calibrated (to within +/- 1 ppm of externally provided reference clock at a single temperature calibration point). If a precisely tuned raw 32.768 kHz crystal oscillator frequency is needed (such as for exporting 32.768 kHz clock to Bluetooth Low Energy device that requires less than a couple hundred ppm of deviation), then external load capacitors need to be added to the PCB just like the traditional method of tuning crystal frequency. In this case, the external load capacitor should be minimized by using a crystal rated for small-load capacitance and the actual external load capacitor should be kept as small as possible (4 pF maximum).
4. Apollo should work with any standard 32.768 kHz tuning fork crystal that meets the above guidelines. Contact Ambiq Support if there is another specific crystal that you would like to use.

[1] No external load capacitors result in a couple hundred ppm error with a 32 kHz clock, which is compensated by a digital calibration to create low-ppm 16 kHz clock for general use and 100 Hz clock for RTC.

3.2.4.2 32 kHz Crystal Calibration during Manufacturing

Apollo has calibration logic which may be used to measure the frequency of an internal clock signal relative to the frequency of an externally provided reference clock. To enable a fast calibration, the reference clock should be between 1 MHz and 10 MHz, and should be a 1 ppm or better reference clock to enable accurate calibration. This reference clock may be input to either GPIO15 or GPIO25, so one of these pins should be made available to test fixture connections to enable calibration during manufacturing flow.

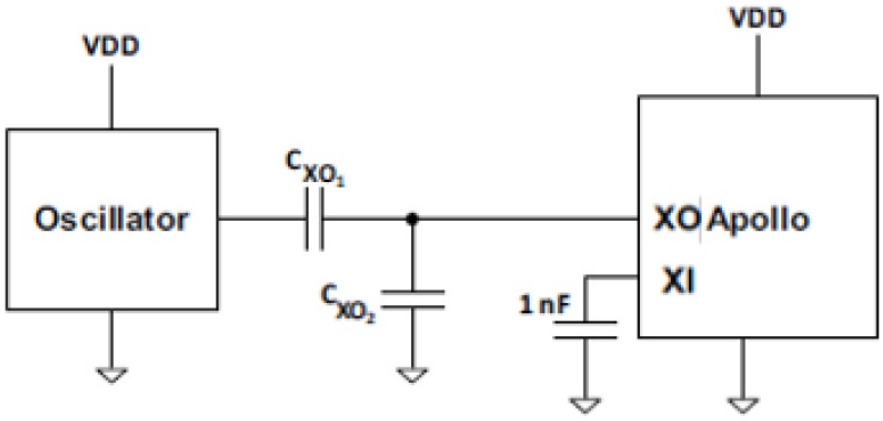
3.2.4.3 External Clock Input to XO/XI

An external 32 kHz clock can be fed into the Apollo XO pin (not XI pin). Due to design requirements, some customers prefer to use an external oscillator (XO) device, or a temperature-controlled external oscillator (TCXO) as a replacement for the 32.768 kHz crystal. The Apollo SoC crystal oscillator was not originally designed to support these kinds of inputs but can be adapted to work with them.

The crystal-controlled oscillator circuit expects an input between 150 and 250 mV peak-to-peak, with a nominal value of 200 mV peak-to-peak. Typically, XO-type devices have a much higher output voltage, and must be AC-coupled into the Apollo oscillator input. To do so, Ambiq recommends using a

capacitive divider between the XO/TCXO output and the XO pin of the device. The XI pin must not be left floating. Instead, a 1 nF capacitor should connect the XI pin to the SoC's ground. See Figure 3-2 for an example of a circuit illustrating the recommended connection.

Figure 3-2: External Oscillator Example Connection



3.3 Reset Design Considerations

3.3.1 Overview

This design guideline describes how to protect from resets caused by spurious pulses from external EMI/crosstalk sources. Any noise spike of sufficient amplitude to instantaneously drop V_{DD} below the V_{IL} threshold, even as short as 200 ps in duration, can cause an unwanted and unexpected reset of the Apollo SoC on nRST.

3.3.2 Applicable Silicon Revisions

This design guideline applies to all versions and packages of Apollo silicon, APOLLO512-xxx.

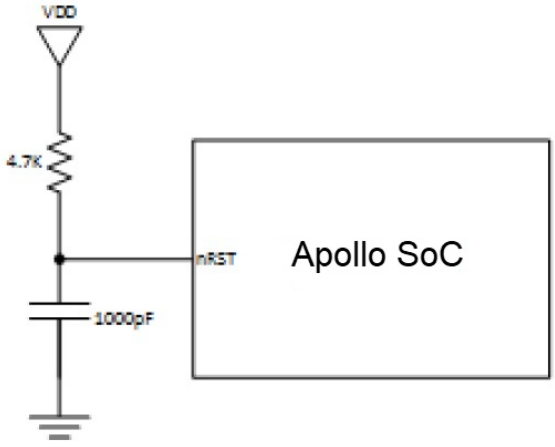
3.3.3 Application Impact

Disruption of normal operation may occur due to unexpected resets caused by spurious noise pulses as short as 200 ps.

3.3.4 Guidelines

The solution for this issue is to add a capacitor between the nRST pin and ground to attenuate/filter such negative voltage incursions, and add a pull-up resistor on the nRST pin. See Figure 3-3 below.

Figure 3-3: Recommended Reset Filter Circuit



The value of the filter capacitor is selected based on the assumption that the rise time and fall time of the spurious signal is 1 ns. A 4.7 kΩ pullup resistor is added to the nRST signal. Assuming a 3.3 V supply, the minimum value for the filter capacitor is determined as follows (to limit ripple on the nRST line to a maximum of 5 mV):

For current, *I*,

$$I = \frac{\text{VDD}}{R} = \frac{3.3\ \text{V}}{4.7\ \text{k}\Omega} \approx 700\ \mu\text{A}$$

and for minimum capacitance, C_{min},

$$Cmin = I \times \frac{1\ ns}{5\ mV}$$

then

$$Cmin \approx 150\ pF$$

While 150 pF will work, 1000 pF is recommended to ensure sufficient filtering in all environments and it is a very common value. For these reset circuit components, consider that an intentional reset pulse should be at least 2 time constants of this R-C combination to ensure that the reset pulse is of sufficient duration below V_{IL}. The time constant, τ, for the above R-C values is 4.7 µs, so a valid reset pulse of at least 15 µs would meet a two time constant guideline, which is recommended. Note that the reset pulse of a typical external debugger is at least 50 µs.

3.4 ADC Input Characteristics

3.4.1 Overview

These design guidelines describe hardware requirements for Apollo ADC inputs.

3.4.2 Applicable Silicon Revisions

These design guidelines apply to all versions and packages of Apollo silicon, APOLLO512-xxx.

3.4.3 Application Impact

Adequate sample-and-hold time must be allowed to enable target conversion accuracy.

3.4.4 Guidelines

3.4.4.1 Calculating Minimum ADC Sample-and-Hold Time

The ADC on the Apollo is a successive approximation register (SAR) ADC with 10 pF input capacitance. If there is large input impedance to the ADC input, then the sample-and-hold time must be increased to ensure the 10 pF sampling capacitor has time to settle.

A rough estimation of time constant is:

Time constant (τ) = Input impedance (kΩ) x ADC input Capacitance (pF)

Assuming no external capacitance on the ADC input, a conservative value of 12 pF (the 10 pF ADC capacitance plus a couple pF for package pin impedance) can be used.

An example calculation for 100 kΩ input impedance (such as if a 200 kΩ resistive divider is used for battery measurement) is:

$$\tau = 100\ k\Omega \times 12\ pF = 1.2\ \mu s$$

The required hold time to guarantee that the capacitance has settled (charged/discharged) to meet target accuracy is:

- 5% accuracy: 3 * 1.2 µs = 3.6 µs
- 1% accuracy: 5 * 1.2 µs = 6 µs
- 10-bit accuracy: 7 * 1.2 µs = 8.4 µs

Apollo allows the sample/hold time to be specified in the number of ADC clocks. If you have ADC configured to use 1.5 MHz ADC clock, then the sample-and-hold setting of 8 cycles provides ~ 5 µs. In this example, if higher than 1% accuracy is required, then the ADC clock would need to be adjusted accordingly.

3.4.4.2 ADC Channel 0 Input Leakage

The Apollo ADC supports 13 user-selectable input channels, eight of which are external GPIO inputs. ADC external inputs 1 through 7 have an input leakage current specification of typically 0.1 nA, with a maximum leakage of 20 nA. ADC external input 0 has a much higher input leakage current, typically 5 µA, but as high as 10 µA.

The additional leakage current on external input 0 can create a noticeable offset in ADC samples, depending on the output impedance of the signal source being measured. Customers using external input 0 must be aware of this additional leakage and account for it when selecting a signal source to be sampled, or use one of the other seven external inputs.

3.5 Debug Connections

3.5.1 Overview

These design guidelines describe hardware design requirements for debugging on an Apollo board.

3.5.2 Applicable Silicon Revisions

These design guidelines apply to all versions and packages of Apollo silicon, APOLLO512-xxx.

3.5.3 Application Impact

Following these recommendations ensures proper connection and reliable operation while debugging the application.

3.5.4 Guidelines

3.5.4.1 SWD Debug Line Termination

It is required to include the following debug signal terminations:

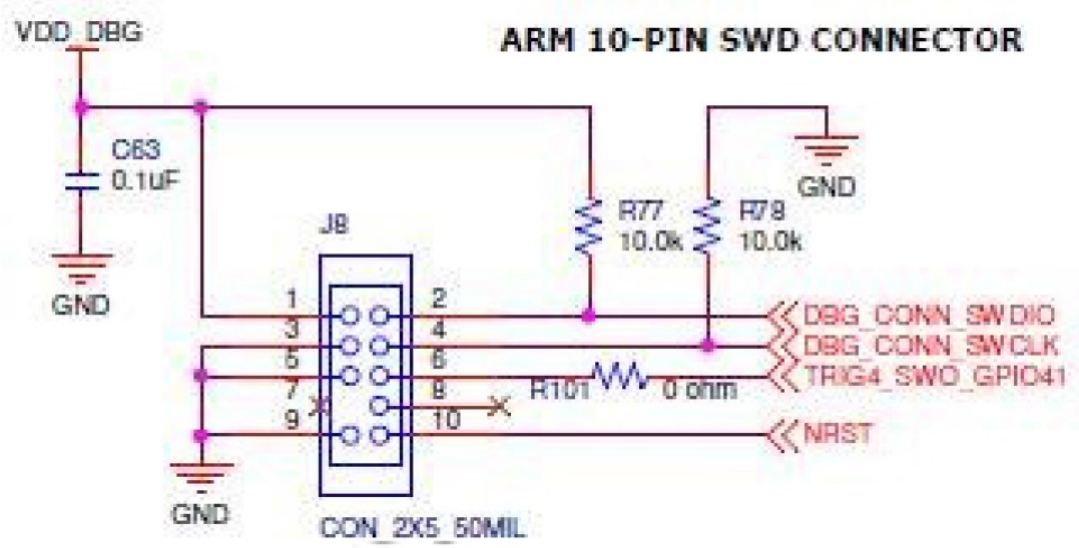
- GPIO20/SWDCK: 10 kΩ pull-down to V_{SS}
- GPIO21/SWDIO: 10 kΩ pull-up to V_{DD}

3.5.4.2 Cortex SWD Debug Connector

As shown in Figure 3-4 on page 19 below, it is recommended to bring DBG_CONN_SWCLK (SWDCK), DBG_CONN_SWDIO (SWDIO), TRIG4_SWO_GPIOI41 (SWO), NRST (nRST), VDD_DBG (V_{DD}) and GND to a debug header to enable full functionality of external Cortex debuggers and flash programmers.

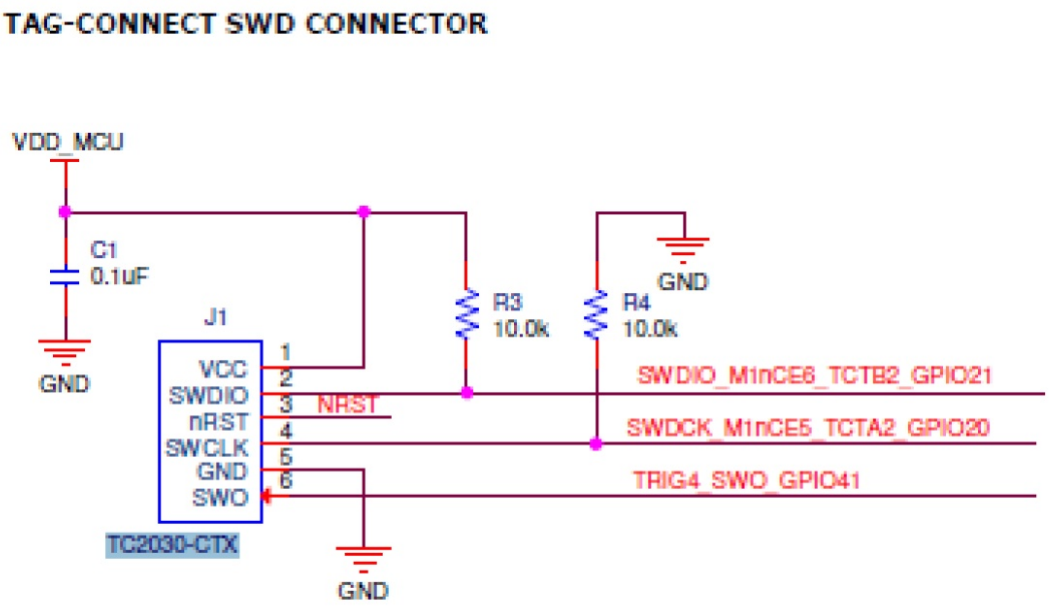
The standard Cortex debug header on the Apollo EVK is useful for boards that are not space constrained. A popular manufacturer is Samsung, and the ordering information for the required header is: Samtec FTSH-105-01

Figure 3-4: Apollo SWD Circuit Using a Standard 2x5 Header



An alternate SWD connector such as Tag-Connect is recommended for more space constrained designs. The TC2030-CTX 6-Pin Cable for Arm® Cortex® (TC2030-CTX) is used for the mini-connector, and its pinout specification is described here: https://www.tag-connect.com/info

Figure 3-5: Apollo SWD Circuit Using a 2x3 Tag Connector



3.6 IOM/IOS Connections

3.6.1 Overview

This design guideline describes hardware design requirements for the IOM and IOS modules.

3.6.2 Applicable Silicon Revisions

This design guideline applies to all versions and packages of Apollo silicon, APOLLO512-xxx.

3.6.3 Application Impact

Following these recommendations ensures proper connection and reliable operation for I^2C and SPI communication in the IOM/IOS modules.

3.6.4 Guidelines

SPI and I^2C Clock Termination

Apollo requires that a 100 Ω series resistor be included in-line with the SPI/I^2C master clock lines (SCK and SCL).

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