DESIGN GUIDELINES

Apollo2 System on Chip

Ultra-Low Power Apollo2 SoC Family

A-SOCAP2-DGGA01EN v1.2

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Revision History

Revision	Date	Description
1.0	February 2017	Initial release
1.1	February 2019	Updated “External 32.768 kHz Clock Input on XO” guideline
1.2	January 5, 2023	Updated document template

Reference Documents

Document ID	Description

Table of Contents

List of Figures

SECTION

1

Introduction

This document is a compilation of detailed design guidelines for the Apollo2 system on chip (SoC).

SECTION

2

Design Guidelines Summary List

A summary of the design guidelines described in this document is listed below. This lists each design guideline by reference number and title, and a link to its detailed information.

SECTION

3

Detailed Design Guidelines

This section contains the design guidelines. Information covered in each design guideline includes at minimum the following:

- **Design Guideline Reference Number and Title** – Lists reference number and title of the design guidelines topic
- **Overview** – Provides an overview of what is addressed in the design guidelines
- **Applicable Silicon Revisions** – Specifies the silicon revisions to which the design guideline applies
- **Application Impact** – Describes the impact of the addressed issue(s) on a user application
- **Guidelines** – Provides details of the design guidelines

3.1 General Power Considerations

3.1.1 Overview

These design guidelines describe device-level power requirements for the Apollo2 SoC. Consult the Electrical Characteristics chapter of the datasheet for operating specifications, and ensure that these specifications are always met.

3.1.2 Applicable Silicon Revisions

These design recommendations apply to all versions and packages of the Apollo2 SoC silicon, AMAPH1KK-xxx.

3.1.3 Application Impact

The power guidelines are intended to ensure reliable low-power operation. Not adhering to these recommendations may result in unnecessary power consumption and, in some cases, unreliable operation of the Apollo2 SoC.

3.1.4 Guidelines

3.1.4.1 Power Supply Decoupling

Minimum required power supply decoupling is:

- 1 µF on V_{DDP}
- 0.1 µF on V_{DDA}
- 0.1 µF on V_{DDH}

Although the minimum decoupling capacitance on V_{DDP} is 1 µF, it is recommended to include a larger capacitor in the range of 2 µF to 10 µF depending on the transient loads in the system. The Apollo2 SoC V_{DDP} input has a maximum allowed slew rate of 2 kV/s, and this extra decoupling capacitance on V_{DDP} may be required if there are high transient loads on the V_{DDP} rail.

This capacitance can be adjusted down to the lowest necessary to prevent the V_{DDP} slew rate from exceeding the 2 kV/s limit for Apollo2 (but should not be reduced below 1 µF).

3.1.4.2 DC-DC Buck - Inductors and Capacitors

Apollo2 SoC features two built-in Buck converters optimized for a low-power environments, featuring ultra-low quiescent current and an integrated power switch. Therefore, only an external inductor and capacitor are needed for each converter to enable very high efficiency power input for the SoC core, SRAM, Flash memory, analog blocks and digital logic.

To ensure best performance across process, voltage and temperature, voltage and temperature, it is recommended to use 1 µF capacitors for both LDO and Buck mode operation. See Figure 3-1 on page 11 below for a Buck converter example schematic.

- 1 µF on VOUT1
- 1 µF on VOUT2

Buck mode operation provides much higher power efficiency in active mode but requires the use of inductors.

The same size and type is recommended for both VOUT1 (core) inductor and VOUT2 (memory) inductor. There is an option for choosing the size and type of

these inductors. If a smaller footprint is required in the design at the expense of slightly higher current draw, then the recommendation is a 0603 SMT package from Taiyo Yuden:

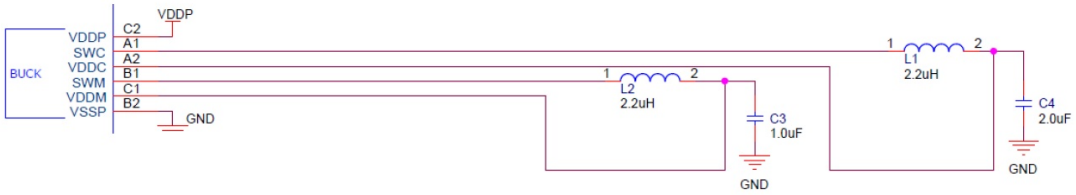
MBKK1608T2R2M
(2.2 µH, .345 Ω, 750 mA current rating, 520 mA saturation current)

If better buck efficiency (up to 5% lower current draw) is needed at the expense of a larger package, then the recommendation is a 0806 SMT package from Bourns:

SRN2010TA-2R2M
(2.2 µH, .145 Ω, 1.2 A current rating, 1.26A saturation current)

If another pair of inductors is selected, it is recommended to ensure 500 mA or higher saturation current for both outputs.

Figure 3-1: Buk Converter Schematic



3.2 32.768 kHz Crystal Selection and Calibration

3.2.1 Overview

These design guidelines outline crystal selection considerations and crystal calibration during manufacturing for on an Apollo2 SoC design.

3.2.2 Applicable Silicon Revisions

These design guidelines apply to all versions and packages of Apollo2 SoC silicon, AMAPH1KK-xxx.

3.2.3 Application Impact

Proper selection of the crystal and design of the crystal circuit should be made to ensure required clock accuracy and reliable operation.

3.2.4 Guidelines

3.2.4.1 32.768 kHz Crystal and Load Capacitors

The Apollo2 SoC clock generator module includes a high-precision crystal-controlled oscillator that works in conjunction with an external 32.768 kHz tuning fork crystal. The crystal oscillator includes a distributed digital calibration function that can be used to calibrate the 16 kHz level of the internal SoC clock divider chain to within ±1 ppm accuracy.

The crystal oscillator is designed to run without the use of external load capacitors, and use the digital calibration function to create a highly accurate clock for internal use. Not using external load capacitors significantly increases oscillator allowance, and allows for a reduction in crystal bias current, which results in lower power consumption. Lower power consumption is often most beneficial when the SoC is in deep sleep mode, but needs to keep the crystal oscillator running as an accurate time source for the RTC module.

The following parameters should be used for the crystal and the crystal circuit:

1. Crystal load capacitance rating: 0 – 12 pF
2. Crystal ESR rating: 0 – 90 kΩ max
3. No external load capacitors on the board

   4 pF or smaller external load capacitor[1] (4.7 pF total external capacitance) if lowppm non-calibrated 32 kHz clock is required.

Crystals which have been tested with the Ambiq crystal circuit are the following:

- Abracon: ABS07-32.768KHZ-7-T, ABS06-32.768KHZ-9-T, ABS25.32.768KHZ-T
- Epson: C-002RX, FC-135, FC-12D, FC-12M
- Microcrystal: CC7V-T1A, CM7V-T1A

All crystals were tested with no external load capacitors.

General Notes:

1. Ambiq typically generates an oscillator allowance of at least 500 kΩ following the guidelines above. Increasing the load capacitance on the XI/XO pins will decrease the oscillator allowance, and using crystals with a higher ESR will reduce the oscillator allowance margin.
2. Common size crystals (3.2 mm x 1.5 mm) generally have a maximum ESR rating of 70 kΩ. The very small 2.0 mm x 1.2 mm crystals generally have a maximum ESR of 90 kΩ, but some crystal vendors, such as Abracon, Epson, or Microcrystal, will have some of the smaller crystals with lower ESR.

[1] No external load capacitors result in a couple hundred ppm error with a 32 kHz clock, which is compensated by a digital calibration to create low-ppm 16 kHz clock for general use and 100 Hz clock for RTC.

3. No external load capacitance is required because the RTC clock source can be digitally calibrated (to within +/- 1 ppm of externally provided reference clock at a single temperature calibration point). If a precisely tuned raw 32.768 kHz crystal oscillator frequency is needed (such as for exporting 32.768 kHz clock to Bluetooth Low Energy device that requires less than a couple hundred ppm of deviation), then external load capacitors need to be added to the PCB just like the traditional method of tuning crystal frequency. In this case, the external load capacitor should be minimized by using a crystal rated for small-load capacitance and the actual external load capacitor should be kept as small as possible (4 pF maximum).
4. Apollo2 SoC should work with any standard 32.768 kHz tuning fork crystal that meets the above guidelines. Contact Ambiq Support if there is another specific crystal that you would like to use.

3.2.4.2 32 kHz Crystal Calibration during Manufacturing

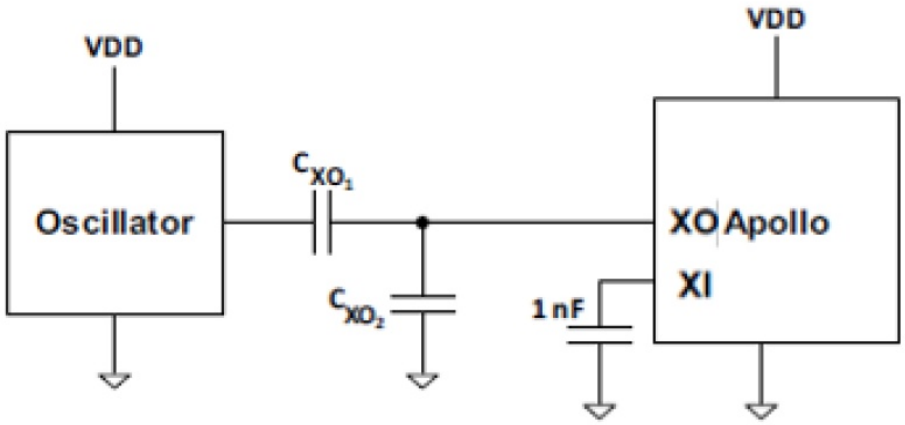
Apollo2 has calibration logic which may be used to measure the frequency of an internal clock signal relative to the frequency of an externally provided reference clock. To enable a fast calibration, the reference clock should be between 1 MHz and 10 MHz, and should be a 1 ppm or better reference clock to enable accurate calibration. This reference clock may be input to either GPIO15 or GPIO25, so one of these pins should be made available to test fixture connections to enable calibration during manufacturing flow.

3.2.4.3 External Clock Input to XO/XI

An external 32 kHz clock can be fed into the Apollo2 XO pin (not XI pin). Due to design requirements, some customers prefer to use an external oscillator (XO) device, or a temperature-controlled external oscillator (TCXO) as a replacement for the 32.768 kHz crystal. The Apollo2 SoC crystal oscillator was not originally designed to support these kinds of inputs but can be adapted to work with them.

The crystal-controlled oscillator circuit expects an input between 150 and 250 mV peak-to-peak, with a nominal value of 200 mV peak-to-peak. Typically, XO-type devices have a much higher output voltage, and must be AC-coupled into the Apollo2 oscillator input. To do so, Ambiq Micro recommends using a capacitive divider between the XO/TCXO output and the XO pin of the device. The XI pin must not be left floating. Instead, a 1 nF capacitor should connect the XI pin to the SoC's ground. See Figure 3-2 on page 14 for an example of a circuit illustrating the recommended connection.

Figure 3-2: External Oscillator Example Connection



3.3 Reset Design Considerations

3.3.1 Overview

This design guideline describes how to protect from resets caused by spurious pulses from external EMI/crosstalk sources. Any noise spike of sufficient amplitude to instantaneously drop V_{DD} below the V_{IL} threshold, even as short as 200 ps in duration, can cause an unwanted and unexpected reset of the Apollo2 SoC on nRST.

3.3.2 Applicable Silicon Revisions

This design guideline applies to all versions and packages of Apollo2 SoC silicon, AMAPH1KK-xxx.

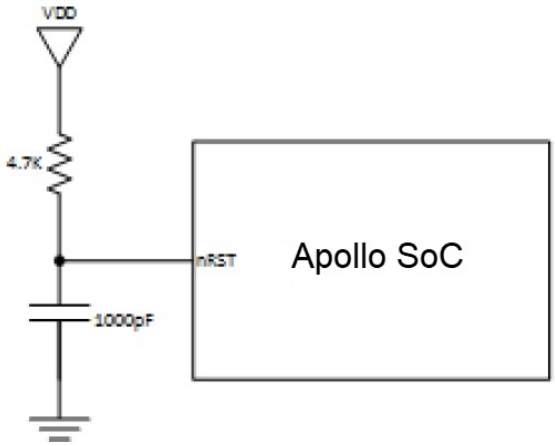
3.3.3 Application Impact

Disruption of normal operation may occur due to unexpected resets caused by spurious noise pulses as short as 200 ps.

3.3.4 Guidelines

The solution for this issue is to add a capacitor between the nRST pin and ground to attenuate/filter such negative voltage incursions, and add a pull-up resistor on the nRST pin. See Figure 3-3 on page 15 below.

Figure 3-3: Recommended Reset Filter Circuit



The value of the filter capacitor is selected based on the assumption that the rise time and fall time of the spurious signal is 1 ns. A 4.7 kΩ pullup resistor is added to the nRST signal. Assuming a 3.3 V supply, the minimum value for the filter capacitor is determined as follows (to limit ripple on the nRST line to a maximum of 5 mV):

For current, *I*,

$$I = \frac{\mathrm{VDD}}{R} = \frac{3.3\ \mathrm{V}}{4.7\ \mathrm{k\Omega}} \approx 700\ \mu\mathrm{A}$$

and for minimum capacitance, C_{min},

$$Cmin = I \times \frac{1\ ns}{5\ mV}$$

then

$$Cmin \approx 150\ pF$$

While 150 pF will work, 1000 pF is recommended to ensure sufficient filtering in all environments and it is a very common value. For these reset circuit components, consider that an intentional reset pulse should be at least 2 time constants of this R-C combination to ensure that the reset pulse is of sufficient duration below V_{IL}. The time constant, τ, for the above R-C values is 4.7 µs, so a valid reset pulse of at least 15 µs would meet a two time constant guideline, which is recommended. Note that the reset pulse of a typical external debugger is at least 50 µs.

3.4 ADC Input Characteristics

3.4.1 Overview

These design guidelines describe hardware requirements for Apollo2 SoC ADC inputs.

3.4.2 Applicable Silicon Revisions

These design guidelines apply to all versions and packages of Apollo2 SoC silicon, AMAPH1KK-xxx.

3.4.3 Application Impact

Adequate sample-and-hold time must be allowed to enable target conversion accuracy.

3.4.4 Guidelines

3.4.4.1 Calculating Minimum ADC Sample-and-Hold Time

The ADC on the Apollo2 is a successive approximation register (SAR) ADC with 4 pF input capacitance. If there is large input impedance to the ADC input, then the sample-and-hold time must be increased to ensure the 104 pF sampling capacitor has time to settle.

A rough estimation of time constant is:

$$\textit{Time constant } (\tau) = \textit{Input impedance } (k\Omega) \times \textit{ADC input Capacitance } (pF)$$

Assuming no external capacitance on the ADC input, a conservative value of 6 pF (the 4 pF ADC capacitance plus a couple pF for package pin impedance) can be used.

An example calculation for 100 kΩ input impedance (such as if a 200 kΩ resistive divider is used for battery measurement) is:

$$\tau = 100\ k\Omega \times 6\ pF = 0.6\ \mu s$$

The required hold time to guarantee that the capacitance has settled (charged/discharged) to meet target accuracy is:

- 5% accuracy: 3 * 0.6 µs = 1.8 µs
- 1% accuracy: 5 * 0.6µs = 3µs
- 10-bit accuracy: 7 * 0.6 µs = 4.2 µs

Apollo2 has a fixed number of ADC clock cycles of 5 cycles for sample-and-hold time. If you have ADC configured to use 1.5 MHz ADC clock, then the sample-and-hold setting of 5 cycles provides ~ 3 µs. In this example, if higher than 1% accuracy is required, then the ADC clock would need to be adjusted accordingly.

3.5 Debug Connections

3.5.1 Overview

These design guidelines describe hardware design requirements for debugging on an Apollo2 SoC board.

3.5.2 Applicable Silicon Revisions

These design guidelines apply to all versions and packages of Apollo2 SoC silicon, AMAPH1KK-xxx.

3.5.3 Application Impact

Following these recommendations ensures proper connection and reliable operation while debugging the application.

3.5.4 Guidelines

3.5.4.1 SWD Debug Line Termination

It is required to include the following debug signal terminations:

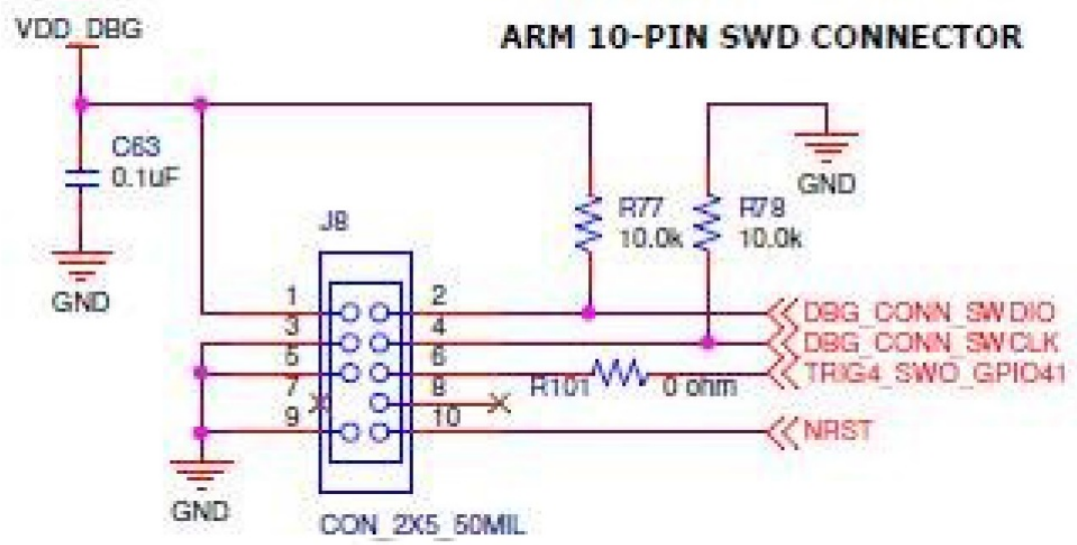
- GPIO20/SWDCK: 10 kΩ pull-down to V_{SS}
- GPIO21/SWDIO: 10 kΩ pull-up to V_{DD}

3.5.4.2 Cortex SWD Debug Connector

As shown in Figure 3-4 on page 18 below, it is recommended to bring DBG_CONN_SWCLK (SWDCK), DBG_CONN_SWDIO (SWDIO), TRIG4_SWO_GPIOI41 (SWO), NRST (nRST), VDD_DBG (V_{DD}) and GND to a debug header to enable full functionality of external Cortex debuggers and flash programmers.

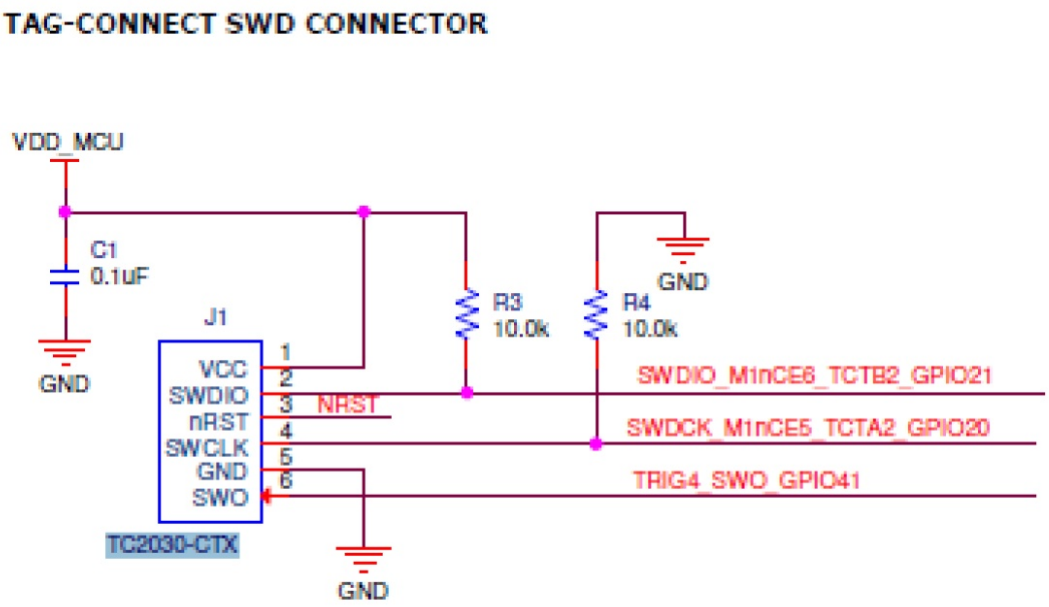
The standard Cortex debug header on the Apollo EVK is useful for boards that are not space constrained. A popular manufacturer is Samsung, and the ordering information for the required header is: Samtec FTSH-105-01

Figure 3-4: Apollo SWD Circuit Using a Standard 2x5 Header



An alternate SWD connector such as Tag-Connect is recommended for more space constrained designs. The TC2030-CTX 6-Pin Cable for Arm® Cortex® (TC2030-CTX) is used for the mini-connector, and its pinout specification is described here: https://www.tag-connect.com/info

Figure 3-5: Apollo SWD Circuit Using a 2x3 Tag Connector



3.6 IOM/IOS Connections

3.6.1 Overview

This design guideline describes hardware design requirements for the IOM and IOS modules.

3.6.2 Applicable Silicon Revisions

This design guideline applies to all versions and packages of Apollo2 SoC silicon, AMAPH1KK-xxx.

3.6.3 Application Impact

Following these recommendations ensures proper connection and reliable operation for I^2C and SPI communication in the IOM/IOS modules.

3.6.4 Guidelines

SPI and I^2C Clock Termination

Apollo2 SoC requires that a 100 Ω series resistor be included in-line with the SPI/I^2C master clock lines (SCK and SCL).

3.7 SPI Master Hardware Design Considerations for 24 MHz Timing and Operation

3.7.1 Overview

This design guideline describes board-level hardware design requirements for Apollo2 SoC SPI master 24 MHz operation. These guidelines should be followed when designing a printed circuit board (PCB) to ensure correct circuit operation of the SPI bus at 24 MHz. Note that 24 MHz SPI master operation is only supported on IOM channels 0 and 4.

3.7.2 Applicable Silicon Revisions

This design guideline applies to all versions and packages of Apollo2 SoC silicon, AMAPH1KK-xxx.

3.7.3 Application Impact

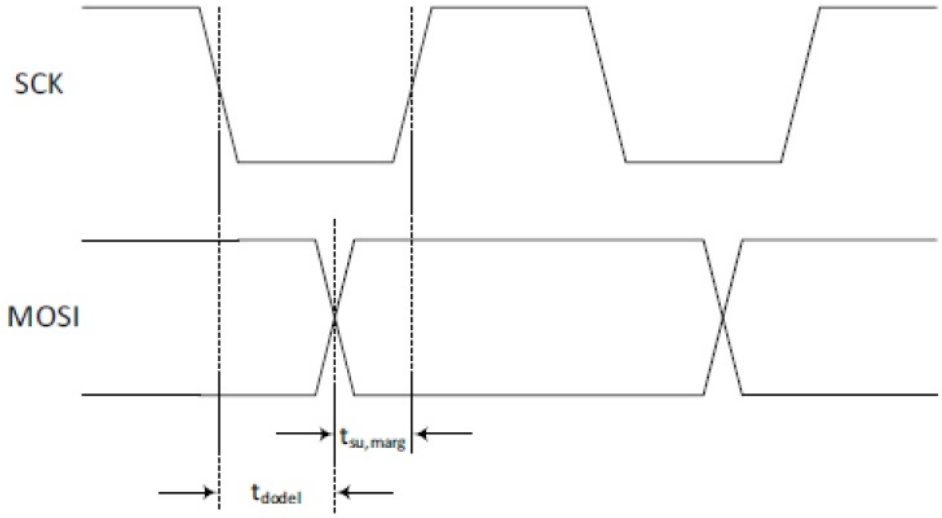
Capacitive loading on SCK and MOSI greater than 20 pF decreases the setup time margin below the acceptable limit for most SPI slave devices when operating at 24 MHz. Because of this, the total capacitive loading on SCK and MOSI must be limited to 20 pF for most applications running SCK at 24 MHz.

Most high speed serial SPI devices that operate at 24 MHz and above have setup times less than about 3 ns and require reduced capacitive loading. However, if the slave device has a setup time requirement that is greater than 3 ns, a series resistor (series termination) on SCK can be added between Apollo2 SoC and the SPI slave device to increase the setup time margin.

3.7.4 Guidelines

One of the critical factors in being able to ensure correct SPI bus operation at 24 MHz between the SPI master and the slave device is ensuring the slave setup time requirements are met. When the data transition edge of the SPI clock occurs, the SPI master device must transition the data output to provide enough setup time margin for the SPI slave device to properly sample the data on the next edge of the SPI clock. Figure 3-6 below illustrates the timing relationship with a SPI bus phase and polarity of 0.

Figure 3-6: Simplified Timing Diagram

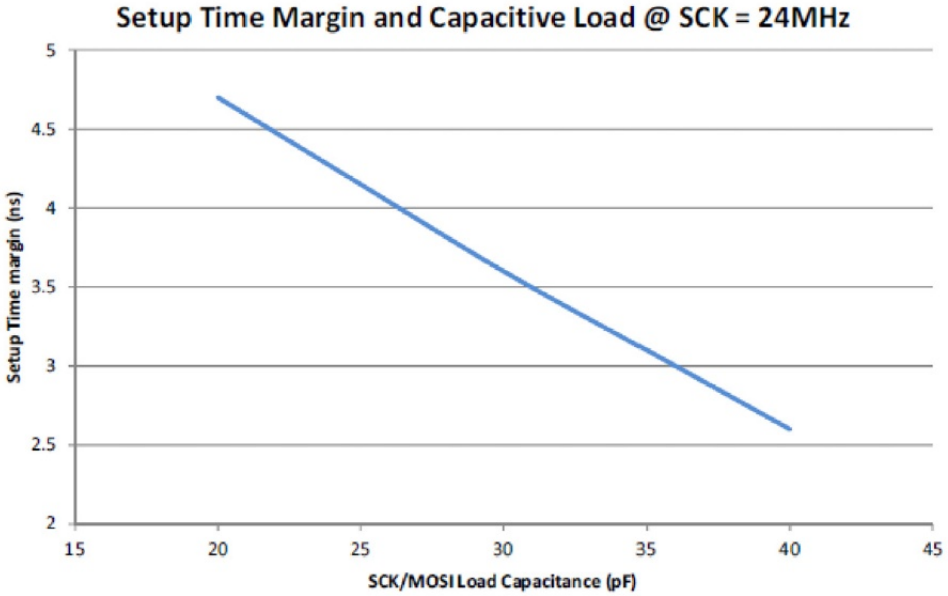


On the falling edge of the SPI clock, the Apollo2 SoC SPI master will transition the data line after a data output delay, t_{dodel}. This delay creates a setup time margin, $t_{su,marg}$, that must be greater than the setup time specification/requirement of the slave device before the next rising edge of the clock when the data is sampled.

The Apollo2 SoC data output delay, t_{dodel}, is dependent upon the drive strength setting of the Apollo2 SCK and MOSI pads and the total capacitive loading of the

signal lines. For 24 MHz operation, the maximum (12 mA) drive strength setting for both SCK and MOSI is required for most applications. Figure 3-7 shows the typical setup time margin, $t_{su,marg}$, achieved with SCK = 24 MHz with maximum (12 mA) drive strength and increasing capacitive load assuming equal capacitive loading and SCK and MOSI.

Figure 3-7: Setup Time Margin at SCK = 24MHz, Various Capacitive Loading

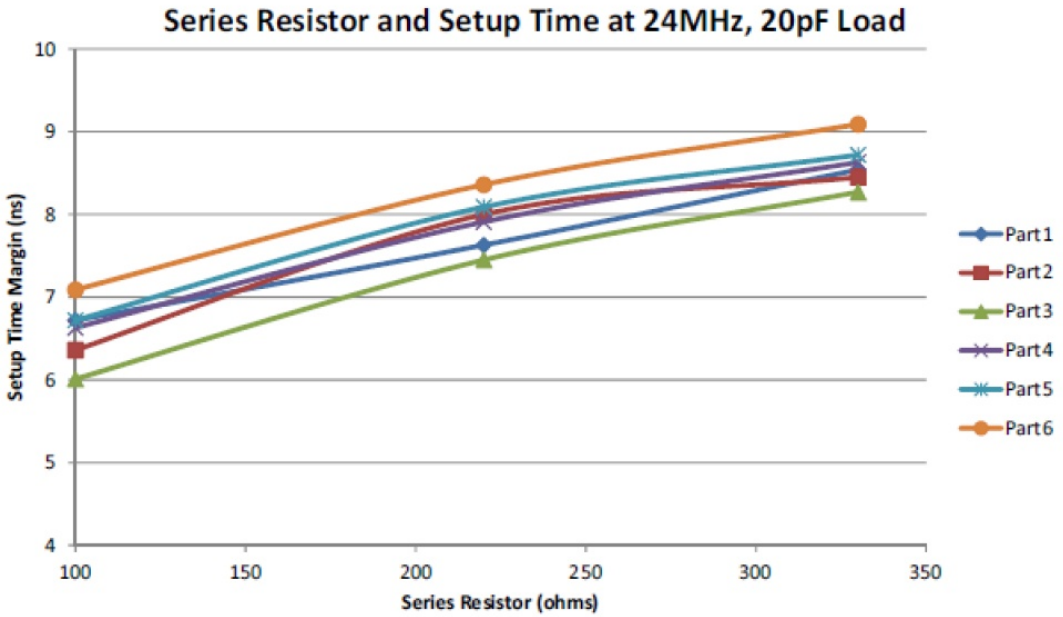


Capacitive loading on SCK and MOSI greater than 20 pF decreases the setup time margin below the acceptable limit for most SPI slave devices2323 when operating at 24 MHz. Because of this, the total capacitive loading on SCK and MOSI must be limited to 20 pF for most applications running SCK at 24 MHz. Note that when probing the SPI bus, the capacitive loading from the oscilloscope probes must be included in the total capacitive loading.

Most high speed serial SPI devices that operate at 24 MHz and above have setup times less than about 3 ns and require reduced capacitive loading. However, if the slave device has a setup time requirement that is greater than 3 ns, a series resistor (series termination) on SCK can be added between Apollo2 and the SPI slave device to increase the setup time margin. It is critical that when the series resistor is added to the SCK line, it must be placed as close as possible to the Apollo2 SCK pin.

Figure 8 shows the setup time margin improvement that can be achieved by adding the series termination resistor on SCK with a 20 pF load on SCK and MOSI at 24 MHz.

Figure 3-8: Setup Time Margin at 24 MHz with Series Resistor and 20 pF Load



The series termination resistor values should not be greater than 330 Ω or the slave VIH and VIL input threshold levels could be violated due to the reduction in clock slew rate. As a general guideline, the series termination resistor values should be kept at 220 Ω or lower and the SPI SCK and MOSI line loading less than 20 pF. Consult the SPI timing diagram in the slave device datasheet to determine the setup time requirement to gauge the setup time margin and potential series termination resistor that will be required.

3.8 External 32.768 kHz Clock Input on XO

3.8.1 Overview

This design guideline describes the recommended external circuit components and SoC pins required to supply an external 32.768 kHz clock to the Apollo2 SoC.

3.8.2 Applicable Silicon Revisions

This design guideline applies to all versions and packages of Apollo2 SoC silicon.

3.8.3 Application Impact

Following these recommendations ensures that the Apollo2 SoC will be clocked reliably and safely with an external clock source.

3.8.4 Guidelines

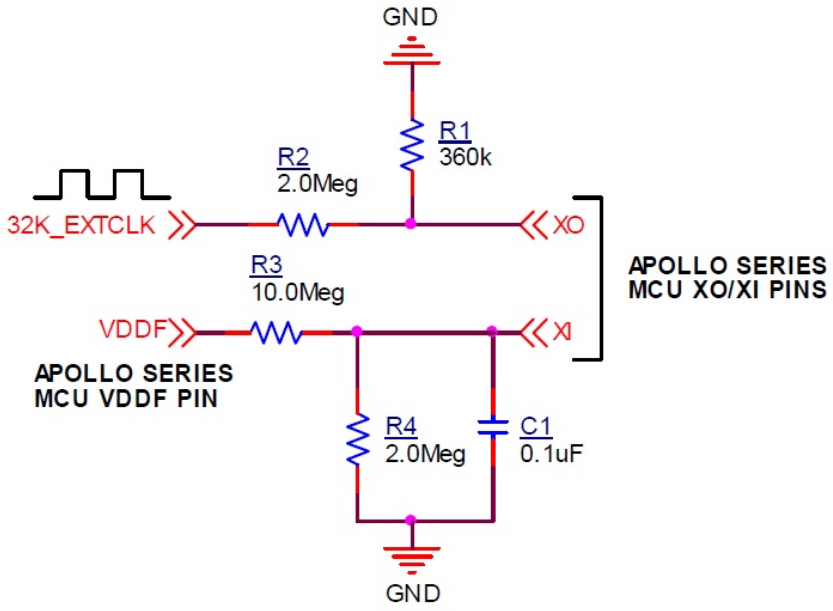
Due to design requirements, some customers prefer to use an external oscillator (XO) device, or a temperature-controlled external oscillator (TCXO) as a replacement for the 32.768 kHz crystal. The Apollo2 SoC's crystal oscillator can be adapted to work with an external clock fed into the Apollo2's XO pin.

There are two requirements to enable external clocking of the SoC - an acceptable clock signal/circuit and correct register configuration.

Clock Signal and Circuit

The crystal-controlled oscillator circuit requires a clock input which meets a specific range of frequency, amplitude and duty cycle. Figure 3-9 shows the recommended circuit diagram, components, and SoC pin connections using a 32.768 kHz external clock (32K_EXTCLK) with peak-to-peak voltage variation allowance from 1.5V to 3.6V.

Figure 3-9: External 32.768 kHz Crystal Clock Circuit Diagram



The recommended circuit must meet the following requirements:

- 32K_EXTCLK:
  - Frequency range: 32.768 kHz external clock source +/- 10% (29.491 - 36.044 kHz). Operation at any frequency above or below this range is not guaranteed.
  - Duty cycle[1]: 45% - 55%
  - Amplitude (Vmin to Vmax peak-to-peak): Vmin = 0V to 0.2V and Vmax = 1.5V to 3.6V

[1] A duty cycle outside of this range has not been validated. It is recommended that the user/designer perform this validation if the clock source cannot meet this duty cycle requirement.

- C1 capacitor
  - Tolerance: 30%
- R1, R2, R3, R4 resistors
  - Tolerance: 10%
  - R3, R4 values cannot be changed if this resistor divider is powered from VDDF
  - R2 value must be between 100 kΩ - 2.0 MΩ.
  - R1, R2 values can be adjusted as long as the XO pin voltage requirements below are met.
- XO pin voltage requirements:
  - Voltage input low range: 0 – 35mV
  - Voltage input peak-to-peak: 340mV (nominal)
  - Voltage input high range: 260mV – 440mV (recommended); 230mV – 600mV (acceptable)
- XI pin voltage requirements:
  - Nominal: 130mV
  - Maximum: 155mV
  - Minimum: 105mV
  - Maximum ripple: 10mV

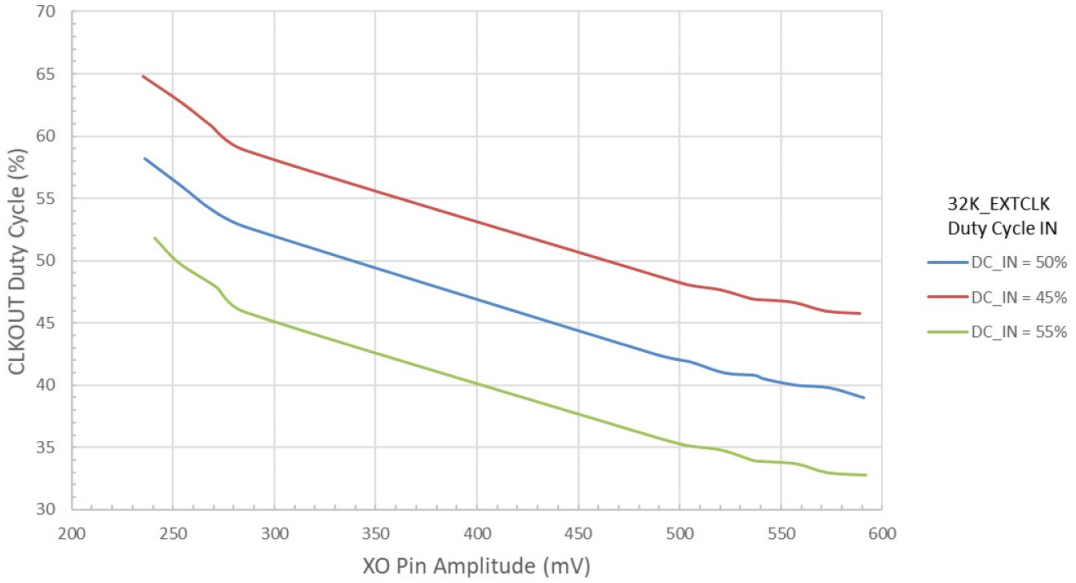
The 32 kHz clock source, 32K_EXTCLK, should be located as close to the XO pin as possible and be routed away from high-switching signals. Trace length should be minimized such that total capacitive load (board + chip pad capacitance) on the XO net should not exceed 5 pF.

NOTE: The user/designer needs to be very careful when probing the net containing the XO pin (output of the resistor divider) and must use a FET probe or similar with ultra-high input impedance (10MΩ or greater) and very low capacitance (1pF or less).

Clock Duty Cycle

Figure 3-10 on page 25 shows the CLKOUT duty cycle variation versus XO pin peak-to-peak voltage for 32K_EXTCLK input duty cycles of 45%, 50%, and 55% with an XI pin bias voltage of 135mV. Under typical conditions, an XO pin peak-to-peak voltage of 340mV will produce a nominal 50% CLKOUT duty cycle with a 50% 32K_EXTCLK input duty cycle.

Figure 3-10: CLKOUT Duty Cycle: XI Pin Voltage = 135 mV



Register Setting

The XTALBIASTRIM and the XTALKSBIASTRIM fields in the MCUCTRL_XTALGENCTRL register, located at address 0x40020124, must set the crystal bias current and the crystal bias kick start current, respectively, to the minimum setting. The XTALGENCTRL register fields are as shown in Table 3-1:

XTALGENCTRL Register
XTAL Oscillator General Control
ADDRESS: 0x40020124

Table 3-1: XTALGENCTRL Register Bits

Bit	Name	Reset	RW	Description
31:14	RSVD	0x0	RO	RESERVED
13:8	XTALKSBIASTRIM	0x1	RW	XTAL IBIAS Kick start trim. This trim value is used during the startup process to enable a faster lock
7:2	XTALBIASTRIM	0x0	RW	XTAL BIAS trim
1:0	ACWARMUP	0x0	RW	Auto-calibration delay control SEC1 = 0x0 - Warmup period of 1-2 seconds SEC2 = 0x1 - Warmup period of 2-4 seconds SEC4 = 0x2 - Warmup period of 4-8 seconds SEC8 = 0x3 - Warmup period of 8-16 seconds

The XTALBIASTRIM and XTALKSBIASTRIM fields must be set to a value of 32 (decimal) for the Apollo2 SoC.

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